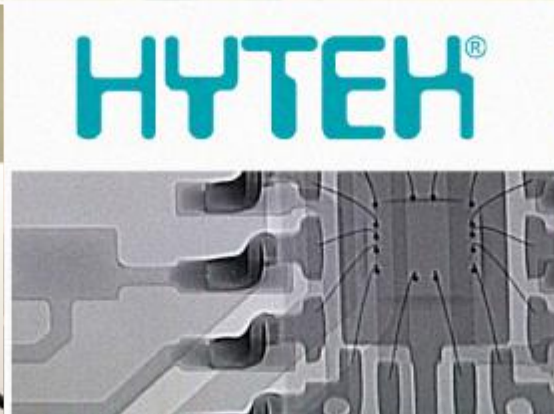

EU HORIZON 2022 FOCUSING

IPC ERFA November 21, 2024

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European Commission

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European Health and Digital Executive Agency (HaDEA)

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Horizon Europe - Space

Boosting the EU's strategic autonomy by supporting technology and research activities in the space domain

Under Horizon Europe Cluster 4 – Space, HaDEA is funding projects that prepare future evolutions of the "EU Space Programme" components (focus on Copernicus and SST) or foster the EU space sector's competitiveness at large, re-inforce its independent capacity to access space or secure its autonomy of supply for critical technologies and equipment.

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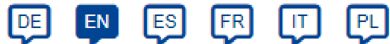
HORIZON EUROPE

Full eurOpean hdi pCb and assembly sUpply chain for Space and INdustrial seGments

FOCUSING



Project description

DE EN ES FR IT PL

Ultra HDI printed circuit board for new satellites

Driven by the miniaturisation of semiconductor packaging, printed circuit boards (PCBs) quickly followed suit, leading to the development of high-density interconnect (HDI) designs. HDI PCB technology and advanced assemblies are crucial for space projects to benefit from the ever-increasing complexity and functionality of modern integrated circuits such as digital signal processors, field programmable gate arrays and other complex devices. This trend is highlighted by the emergence of the system-in-package (SiP) method for space applications. Considering the pivotal role of HDI PCB designs in the satellite sector, the EU-funded FOCUSING project aims to develop cutting-edge electronic devices employing HDI technology across the full European supply chain, from material manufacturing to PCB delivery. The aim is to significantly improve the performance of space equipment.

Show the project objective

Fields of science

engineering and technology > mechanical engineering > vehicle engineering > aerospace engineering > **satellite technology**

Project Information

FOCUSING
Grant agreement ID: 101082236

DOI
10.3030/101082236

EC signature date
10 October 2022

Start date
1 December 2022

End date
30 November 2025

Funded under
Digital, Industry and Space

Total cost
€ 2 712 954,75

EU contribution
€ 2 712 954,25

Coordinated by
IMT SRL
Italy

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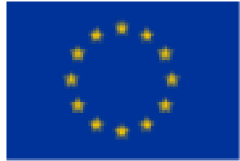

HORIZON EUROPE - 2022

FULL EUR**O**PEAN HDI P**C**B AND ASSEMBLY S**U**PPLY CHAIN FOR **S**PACE AND **IN**DUSTRIAL SE**G**MENTS (FOCUSING)

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Overview

→ TV1: Embedded SiP for Power Supply

→ TV3: Build-up substrate for SiP
→ 6-N-6 / RG740M-Core MEGTRON 7N

Naked substrate

SiP RF Substrate equiped with parts

→ TV2: Build-up substrate for SiP
→ 6-N-6 / RG740-Core Megtron 6

Naked substrate

→ TV4: HDI PCB mother Board
→ 6-N-6 MEGTRON 6

→ DEMO 1: Digital SiP

→ DEMO 3: RF SiP

→ DEMO 2: Digital SiP on PCB HDI mother

→ DEMO 4: RF Sip on PCB HDI mother Board

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ECSS-Q-ST-70-60C test flow for PCB

- PCB qualification – 3 PCBs and test pattern having passed incoming inspection flow for procurement
- PCB qualification – 3 PCBs – Test pattern: A, A/B, AB1, AB12, P, H, X, IST, K, Comb, CAF
  - Optional spare PCB – PCB
  - Visual inspection and non-destructive tests – Group 1
    - Visual inspection – All PCBs / test pattern
      - Impedance test – Custom coupon
      - Dielectric constant/ loss tangent for RF material – Custom coupon
    - Dimensional verification – All PCBs / test pattern
    - High resistance elctrical test – All PCBs / test pattern
    - Cleanliness – PCB#1
    - Warp &twist – All PCBs

- Miscellaneous tests – Group 2
  - Flexural fatique – X
  - Bending test – Rigid Flex
  - Coating adhesion – P
  - Analysis of SnPb coating – P
  - Flammability – K
  - Offgassing – K
  - Outgassing – K
  - Thermal analysis – K
  - Peel strenght – P
  - Solderability test – A/B

- Thermal stress and as received – Group 3
  - Rework simulation – A/B, AB1, AB12
  - Solder bath float – PCB#1, A/B, AB1, AB12
  - Microsection after thermal stress – PCB#1, A/B, AB1, AB12
  - Microsection as received – PCB#1, A/B, AB1, AB12
  - Interconnect stress Test – IST

- Assembly and life test - extended – Group 4
  - Insulation resistance – A/H
  - Dielectric withstanding voltage – A/H
  - Reflow simulation – PCB#2&3 + A, H, P
  - Rework simulation – PCB#2&3
  - Thermal cycling (500cycles@-55/ +100°C) – PCB#2&3 + A, H, P
    - Peel strenght – P
    - Insulation resistance – A/H
    - Dielectric withstanding voltage – A/H
    - Microsectionning – PCB#2&3

- ECM test – Group 5
  - CAF – CAF pattern
    - Reflow simulation – CAF pattern
    - Temperature Humidity Bias – CAF pattern
    - Microsectionning – CAF pattern
  - THB – Comb pattern
    - Reflow simulation – Comb pattern
    - Temperature Humidity Bias – Comb pattern
    - Microsectionning – Comb pattern

- Assembly and life test - short – Group 6
  - Reflow simulation – PCB
  - Rework simulation – PCB
  - Thermal cycling (200cycles@-60/ +140°C) – PCB
  - Microsectionning – PCB

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Example of test plan at HYTEK

Focusing TV4 - 2402a-c				
2402a Group 1 test according to ECSS-Q-ST-70-60C				
Test Step				**Remarks**
Incoming inspection	Microscopy			
Cleanliness §9.3.6	Cleanliness test			
Visual inspection §9.3.1 and §9.3.2	Visual inspection - general and qualitative aspects			
Dimensional verification§9.3.3.1	Visual inspection for dimensional verification			
Warp test§9.3.3.2	Warp test			
Twist test §9.3.3.3	Twist test			
Impedance test §9.3.4				No coupons
2402a Group 2 test according to ECSS-Q-ST-70-60C				
Peel Strength test §9.4.2	Compliance with §9.4.2.k			
Coating adhesion §9.4.5	Tape test			
Thermal analysis §9.4.8	TMA test			
Solderability test §9.4.11				
2402a Group 3 test according to ECSS-Q-ST-70-60C §9.5				
Pre-conditioning / baking §9.2.2	120℃ / min 8 hours			
Rework simulation test §9.5.4	4 PTH holes or pads covering via holes			
Microsectioning	Prepare for microsec.			
Evaluation				
Solder bath float §9.5.3	Float it for 10 s in a solder bath for 288°C x3			
Microsectioning	Prepare for microsec.			
Evaluation				
As is	Area similar to part used for Solder bath float			
Microsectioning	Prepare for microsec.			
Evaluation	Moulding of items			
Interconnect stress test §9.5.5				
2402b Group 4 test according to ECSS-Q-ST-70-60C §9.6				
Pre-conditioning / baking §9.2.2	120°C / min 8 hours			
Insulation Resistance test §9.6.3				
Dielectric withstanding §9.6.4				
Reflow simulation §9.8.3	Vapour phase reflow. 230 °C x2			
Rework simulation test §9.5.4 PTH	350°C 10 x			
Rework simulation test SMD	Hot Air 245°C 2 x			
Thermal cycling §9.8.4	Temp. -55 to +100°C at max. 10°C/min. 500 cycles			
Insulation Resistance test §9.6.3				
Dielectric withstanding §9.6.4				
Peel Strength Test §9.4.2				
Microsectioning 250 Cycles	Prepare for microsec.			
Microsectioning 500 Cycles	Prepare for microsec.			
Evaluation				

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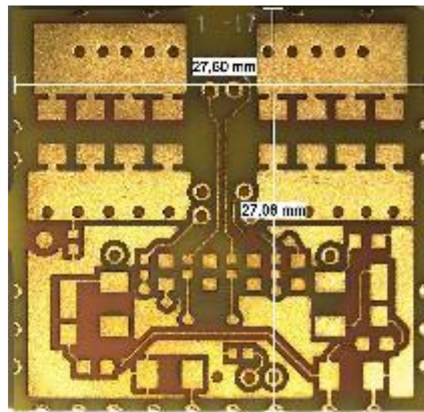
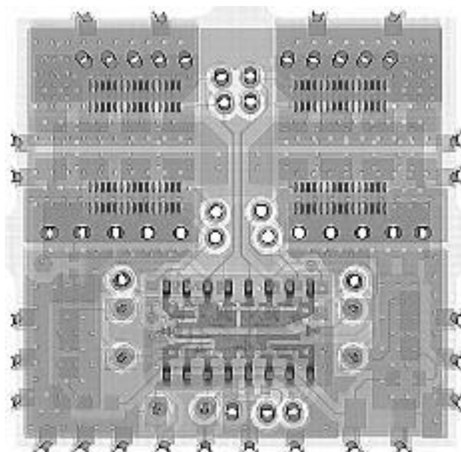
TV1 Embedded components substrate

Test results ECSS-Q-ST-70-60C Group 1 (Example)





Test definition	ECSS-Q-ST-70-60C	Results	Report
Group 1 - Cleanliness	§9.3.6	Compliance	2415a

Tested according to ECSS-Q-ST-70-60C §9.3.6 / IPC TM650 – 2.3.25.1

Conclusion:

The test result show measurement below 1,56µg NaCl eq /cm^2, and is in compliance with ECSS-Q-ST-70-60C §9.3.6

Test definition	ECSS-Q-ST-70-60C	Results	Report
Group 1 - Visual inspection	§9.3.1/2	Compliance	2415b
Group 1 - Dimensional verification	§9.3.3	Have to be verified	2415b

Group 1 Visual inspection - general and qualitative aspects §9.3.1 and §9.3.2

Conclusion:

Compliance with ECSS-Q-ST-70-60C.

Group 1 - Visual inspection for dimensional verification §9.3.3

Conclusion:

Patterns measured – have to be verified according to procurement specification.

Test definition	ECSS-Q-ST-70-60C	Results	Report
Group 1 - Warp	§9.3.3.2	Compliance	2415c
Group 1 - Twist	§9.3.3.3	Compliance	2415c

Conclusion:

Group 1 Warp test show **Compliance** with ECSS-Q-ST-70-60C §9.3.3.2.h + note 1
Group 1 Twist test show **Compliance** with ECSS-Q-ST-70-60C §9.3.3.3.h + note 1

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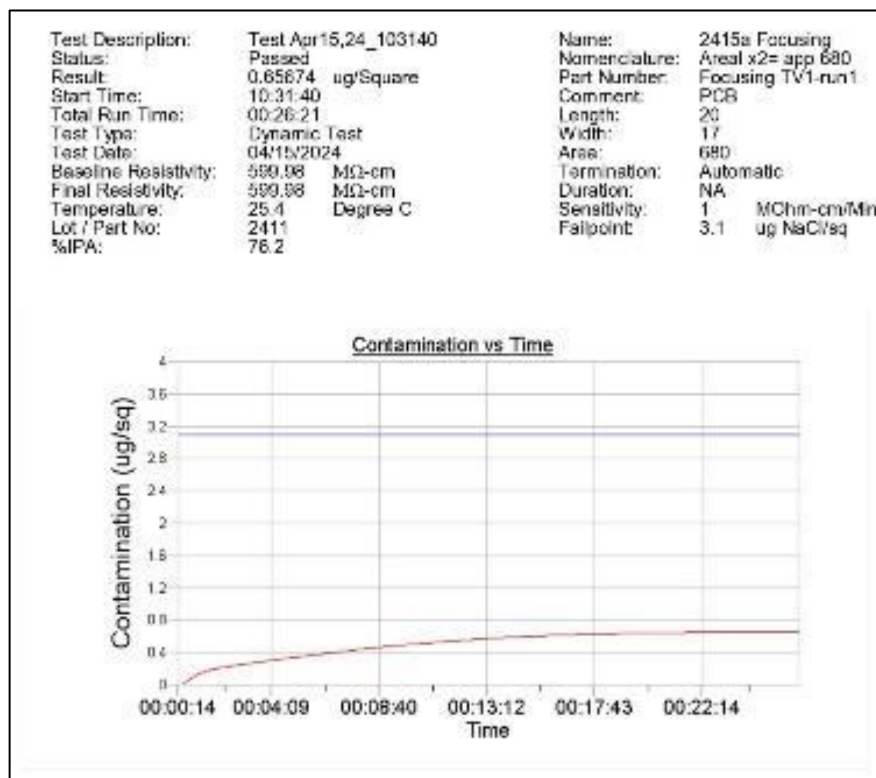
TV1 Embedded components substrate

Test results ECSS-Q-ST-70-60C Group 1 (Example)

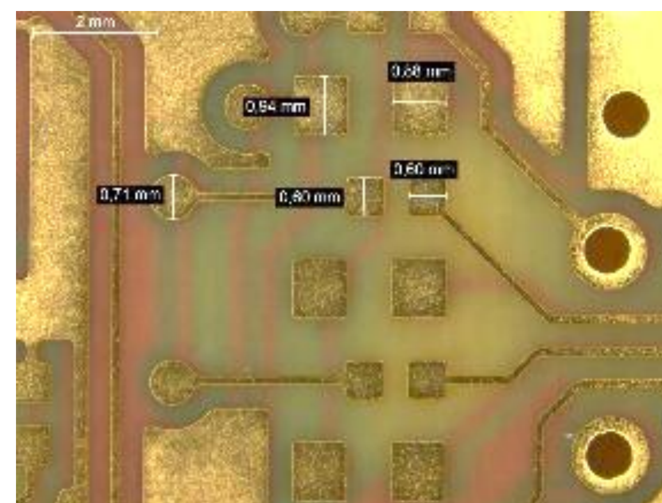
Cleanliness



Test Description:	Test Apr15,24_103140	
Status:	Passed	
Result:	0.65674	ug/Square
Start Time:	10:31:40	
Total Run Time:	00:26:21	
Test Type:	Dynamic Test	
Test Date:	04/15/2024	
Baseline Resistivity:	599.98	MΩ-cm
Final Resistivity:	599.98	MΩ-cm
Temperature:	25.4	Degree C
Lot / Part No:	2411	
%IPA:	76.2	

Name:	2415a Focusing	
Nomenclature:	Areal x2= app 680	
Part Number:	Focusing TV1-run1	
Comment:	PCB	
Length:	20	
Width:	17	
Area:	680	
Termination:	Automatic	
Duration:	NA	
Sensitivity:	1	MOhm-cm/Min
Failpoint:	3.1	ug NaCl/sq

Dimensions



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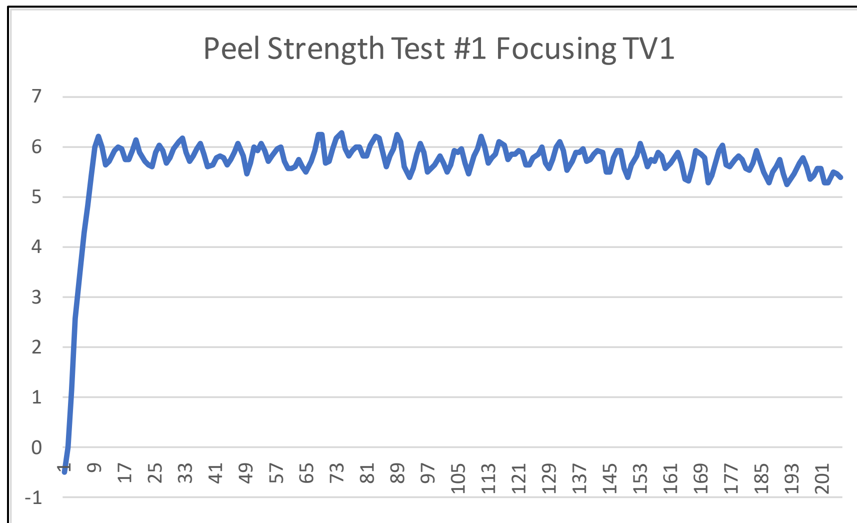
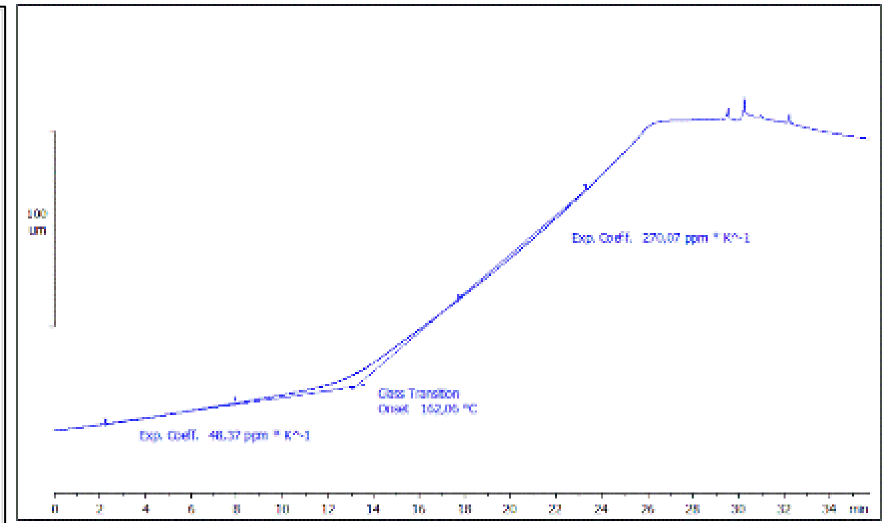
TV1 Embedded components substrate

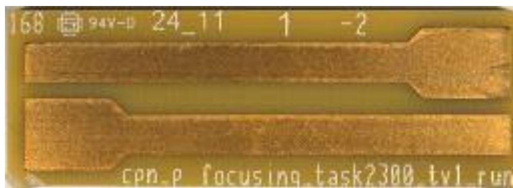
Test results ECSS-Q-ST-70-60C Group 2 (Example)

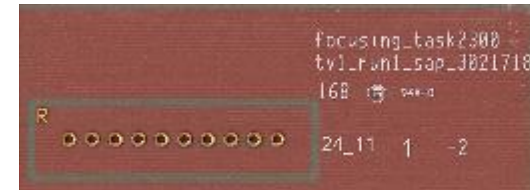
Peel strength



TMA (CTE/TG)







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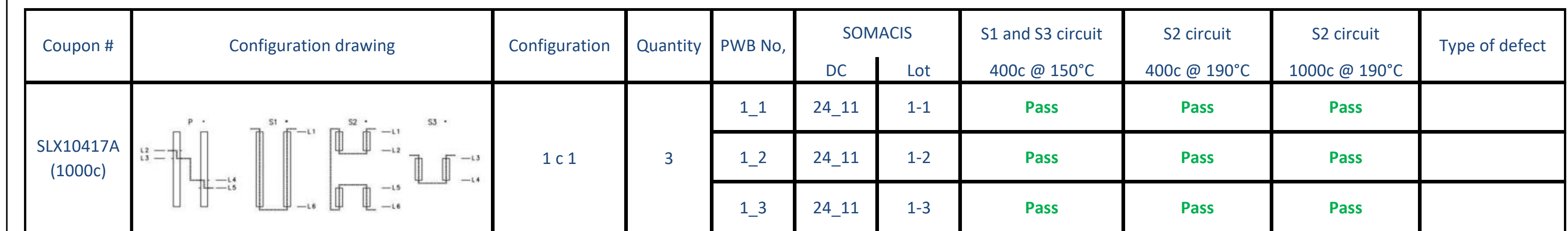
TV1 Embedded components substrate

Test results ECSS-Q-ST-70-60C Group 3 (Example)

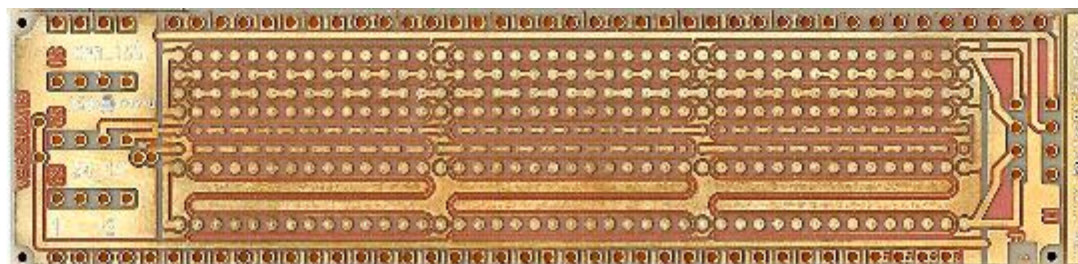
Test definition	ECSS-Q-ST-70-60C	Results	Report
Group 3 – Interconnect stress test (IST)	§9.5.5	Compliance	PWB

Conclusion:

Interconnect stress test (IST) showed compliance on all configurations.



Coupon #	Configuration drawing	Configuration	Quantity	PWB No,	SOMACIS DC	SOMACIS Lot	S1 and S3 circuit 400c @ 150°C	S2 circuit 400c @ 190°C	S2 circuit 1000c @ 190°C	Type of defect
SLX10417A (1000c)		1 c 1	3	1_1	24_11	1-1	Pass	Pass	Pass	
				1_2	24_11	1-2	Pass	Pass	Pass	
				1_3	24_11	1-3	Pass	Pass	Pass	



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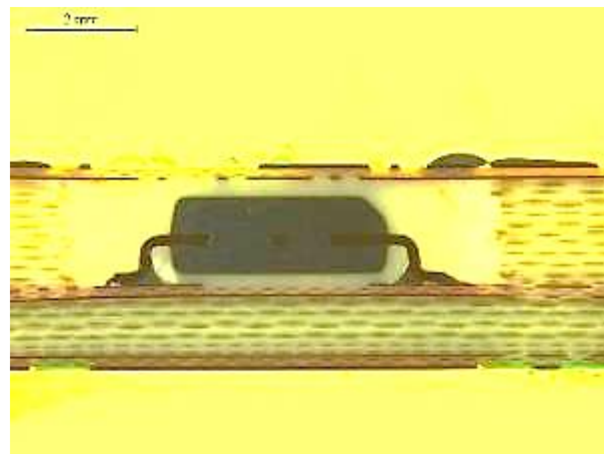
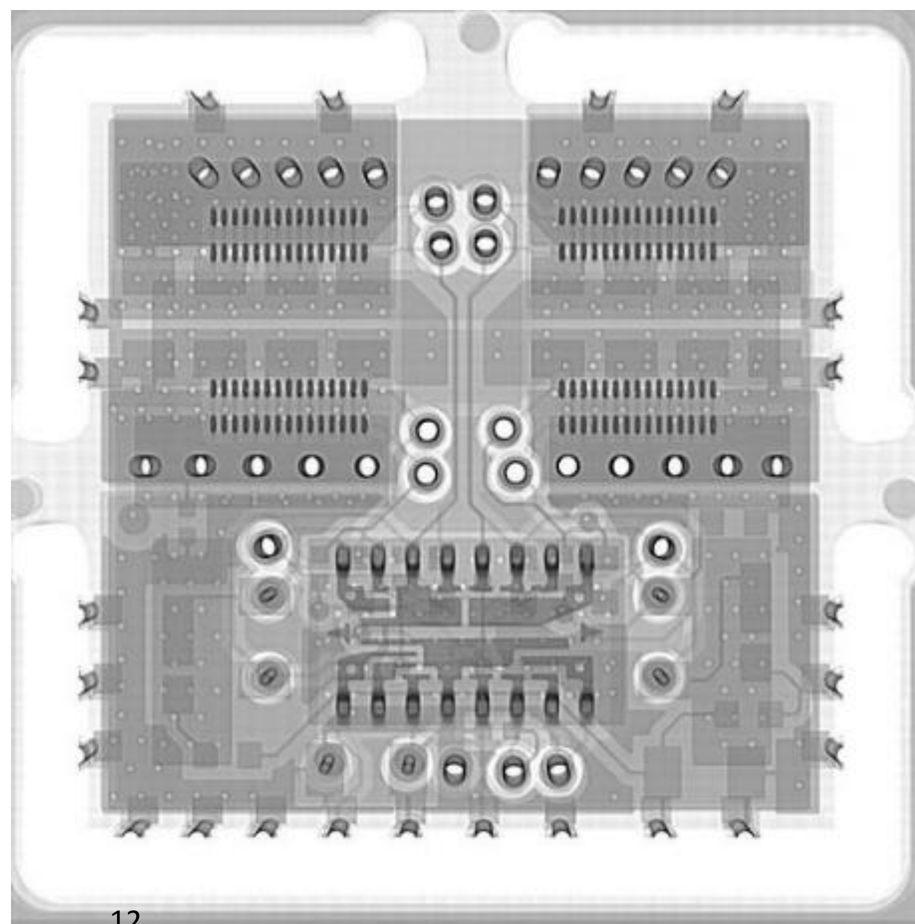
TV1 Embedded components substrate

Test results ECSS-Q-ST-70-60C Group 4 (Example)

Microsectioning



X-ray



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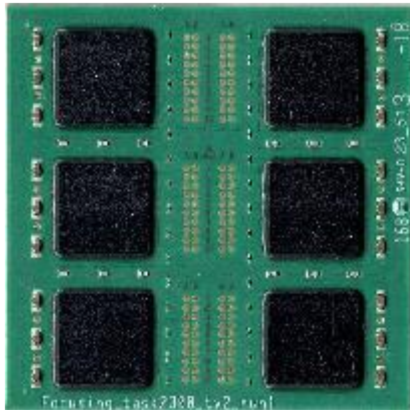
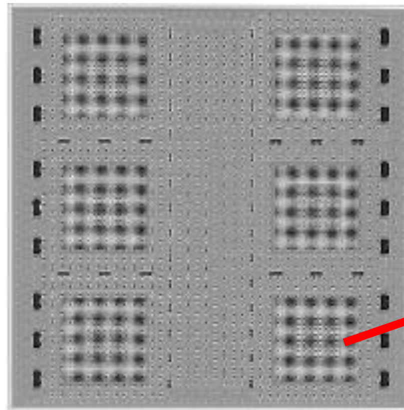
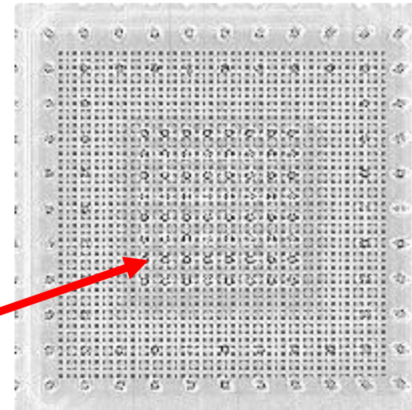
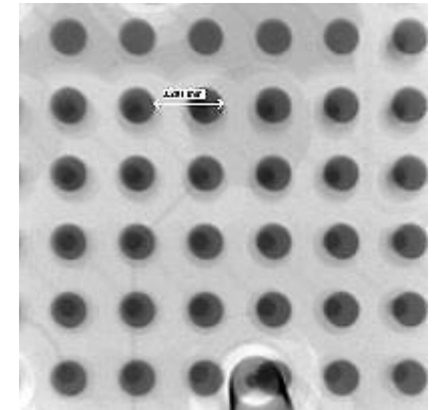
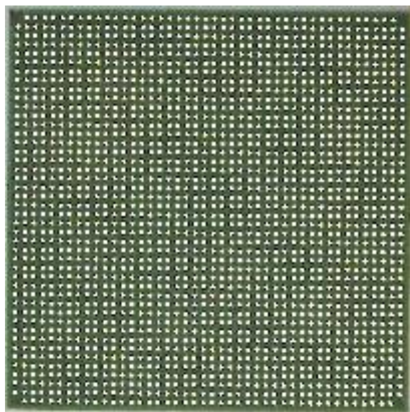
TV2 Digital SiP



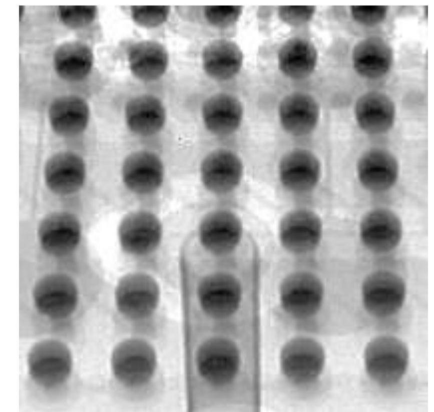








BGA 40 X 40 mm 1932 I/O
Pitch 1 mm
Flip Chip 10 X 10 mm 2116 I/O
Pitch 0.2 mm



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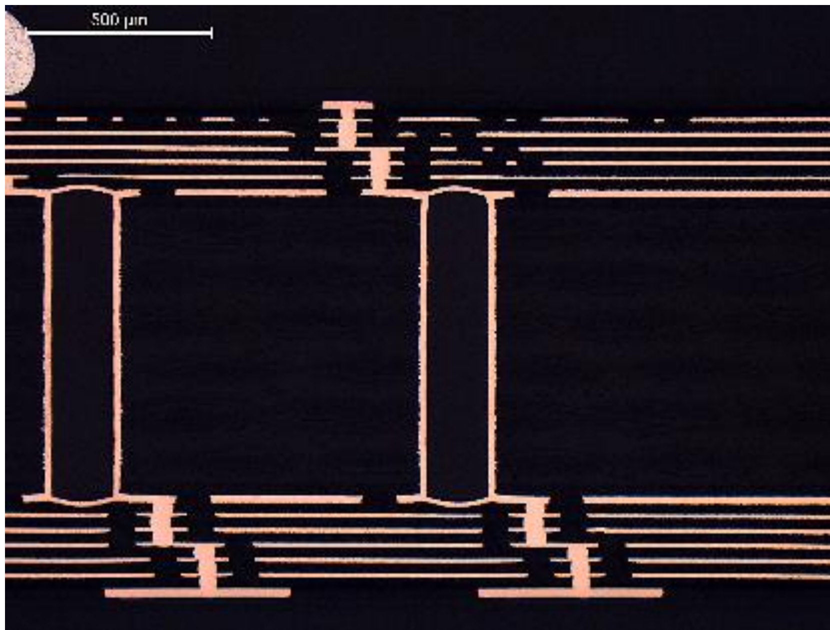
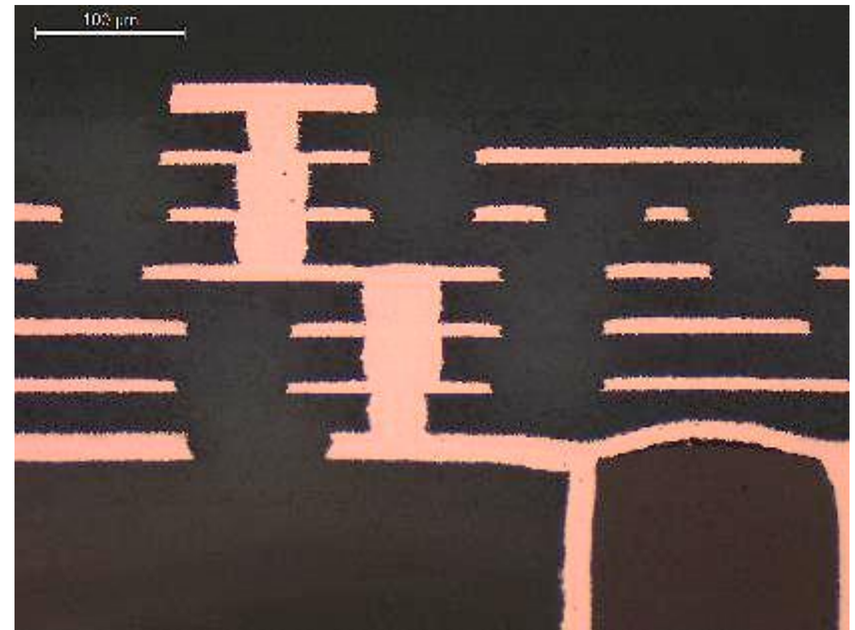
TV2 Digital SiP substrate

Test results ECSS-Q-ST-70-60C Group 4 (TC250)





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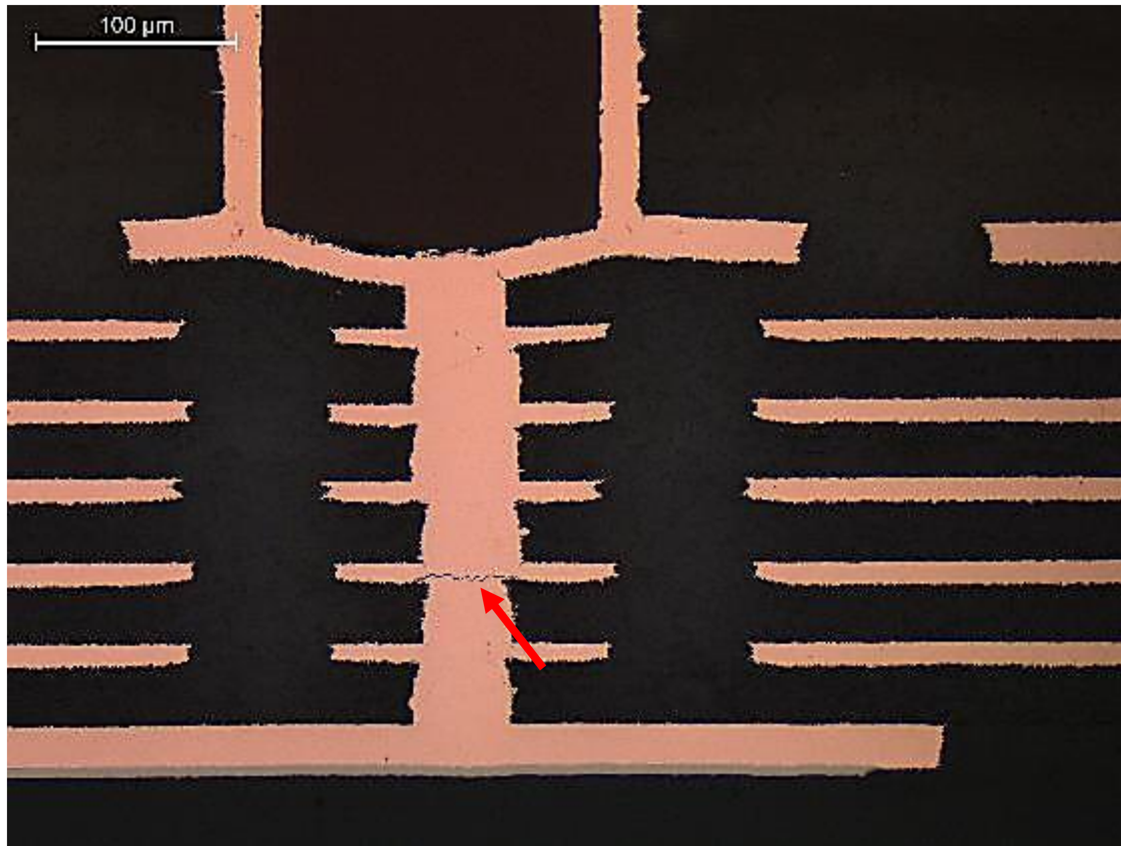
TV2 Digital SiP substrate

Test results ECSS-Q-ST-70-60C Group 4 (TC500)



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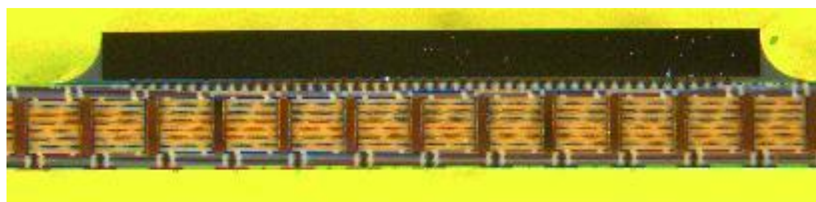
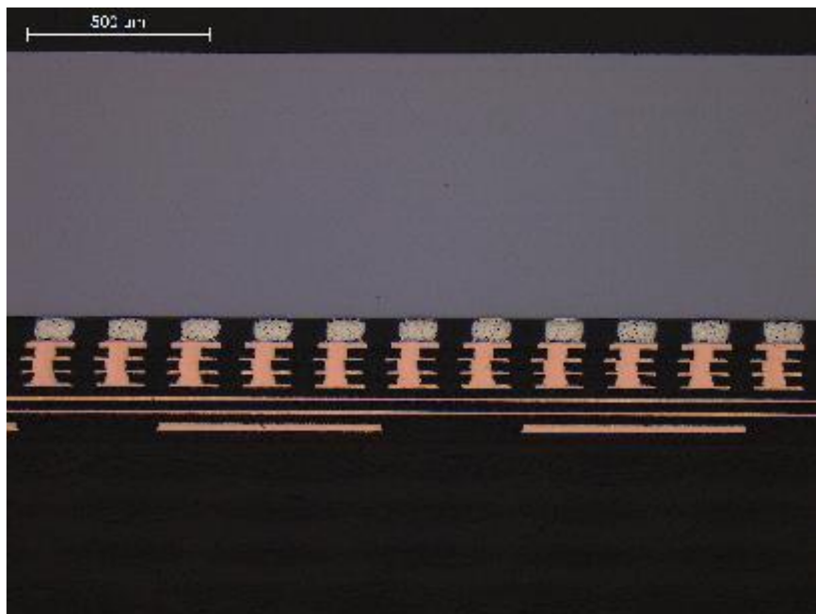
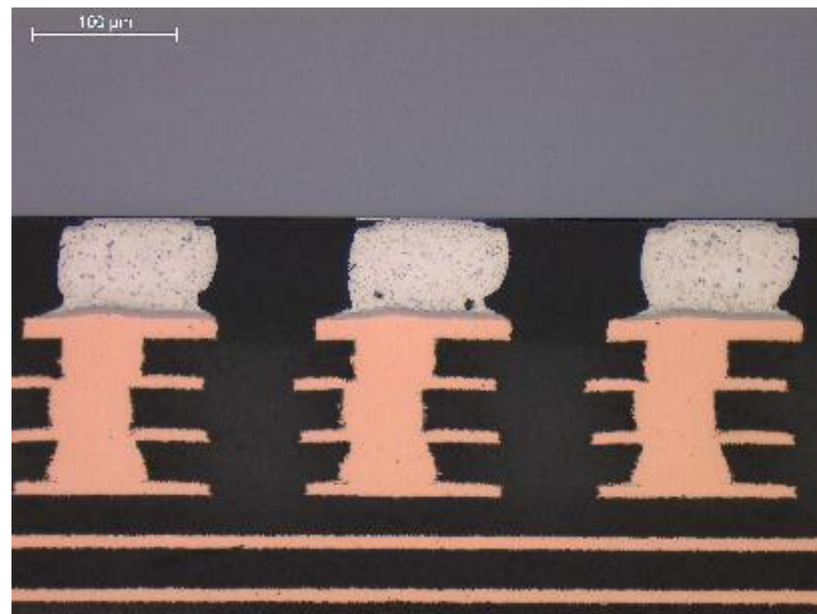
TV2 Digital SiP

Test results ESCC-2566000 (TC500)







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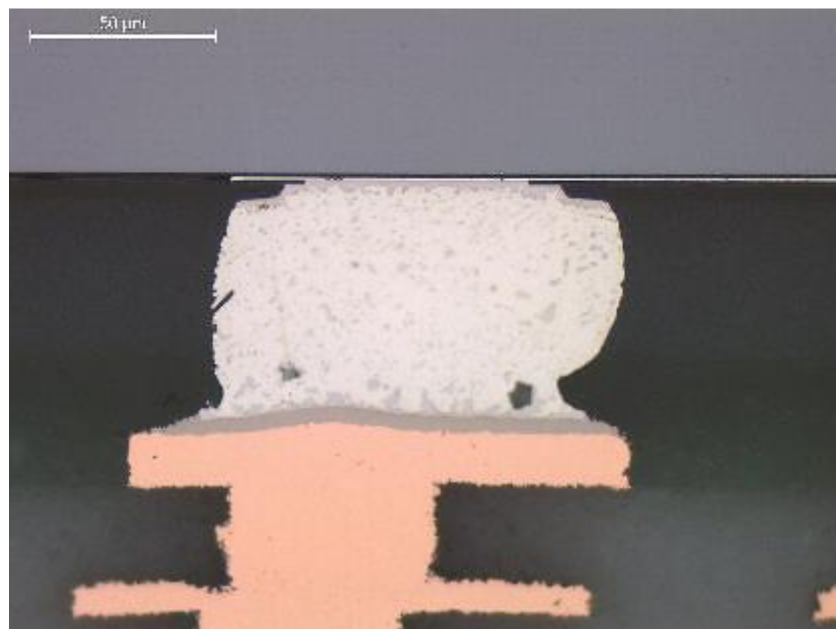
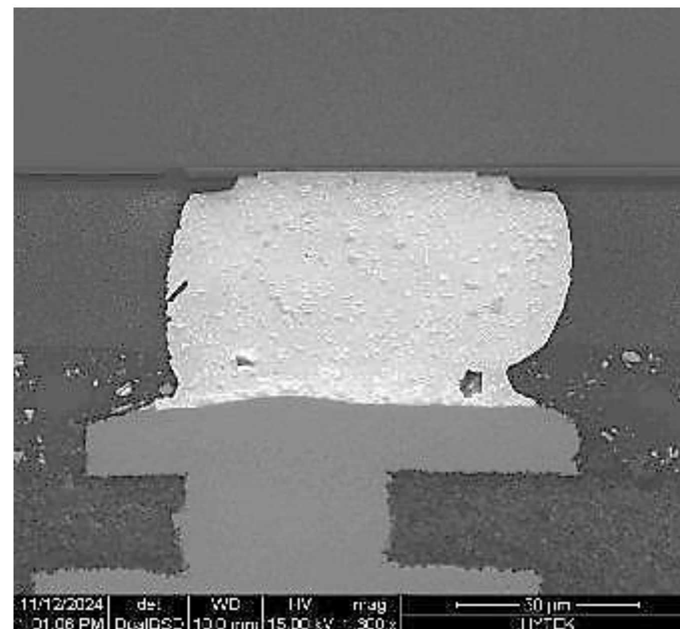
TV2 Digital SiP

Test results ESCC-2566000 (TC500)

Microscopy



ESEM



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TV4 PCB

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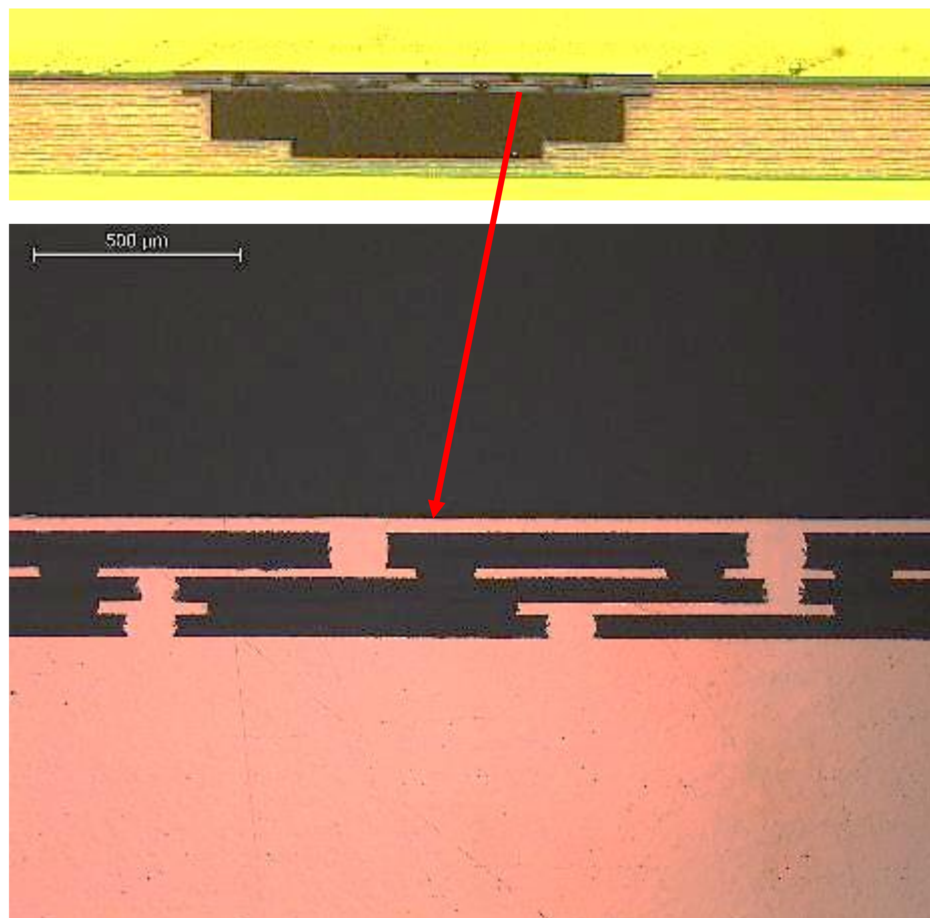
TV4 PCB

Test results ECSS-Q-ST-70-60C Group 4 (Cu Coin after TC500)



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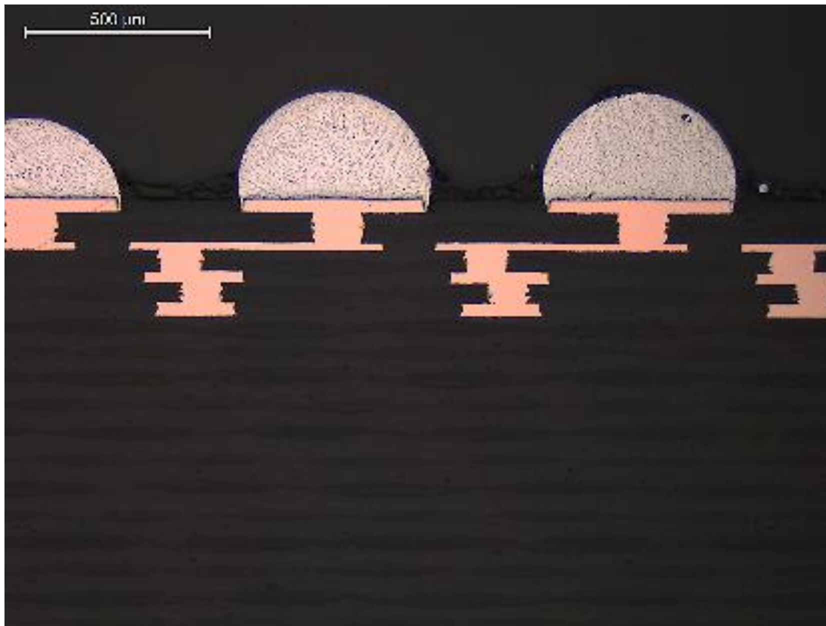
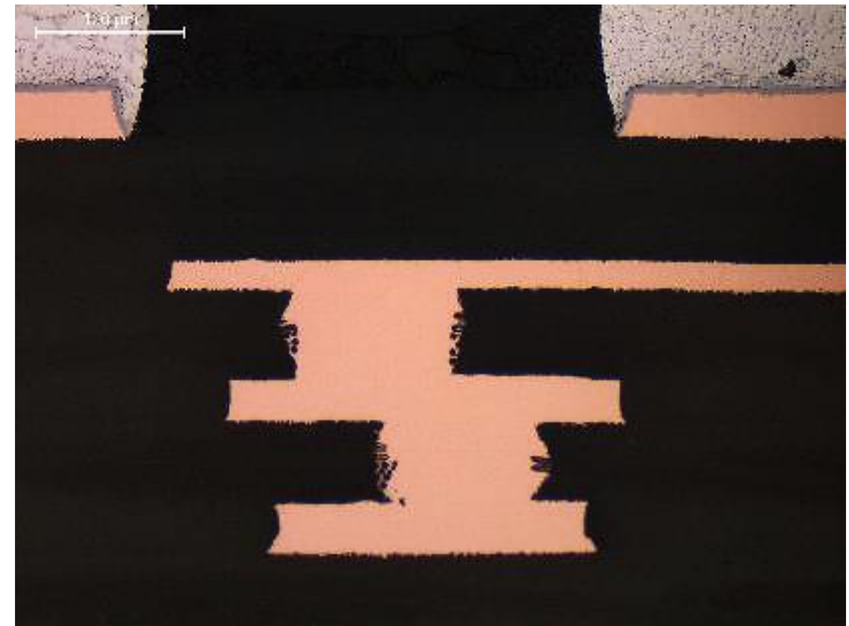
TV4 PCB

Test results ECSS-Q-ST-70-60C Group 4 (TC500)





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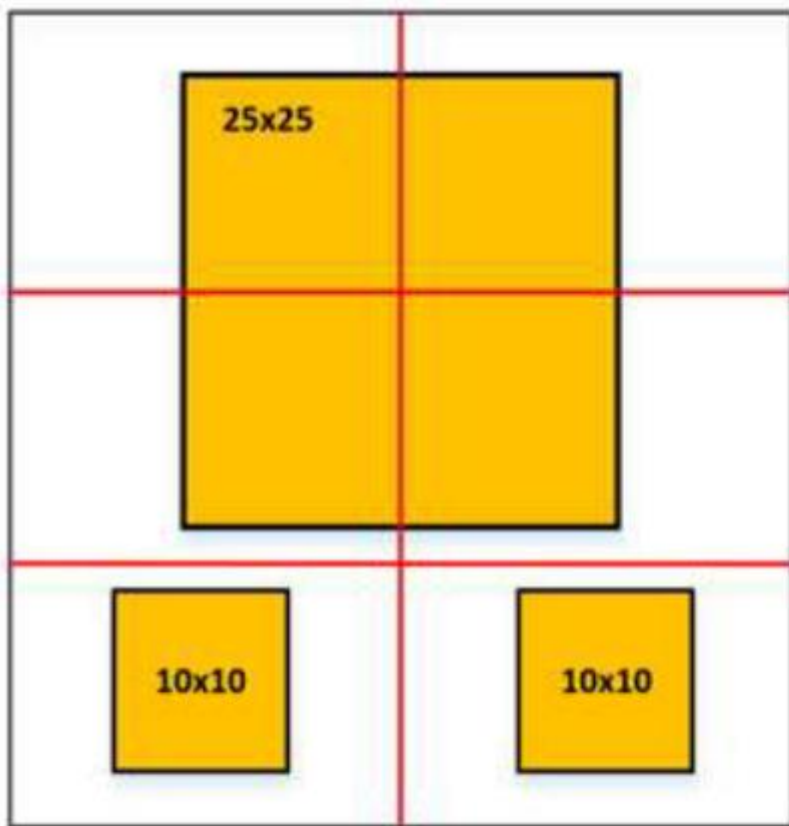
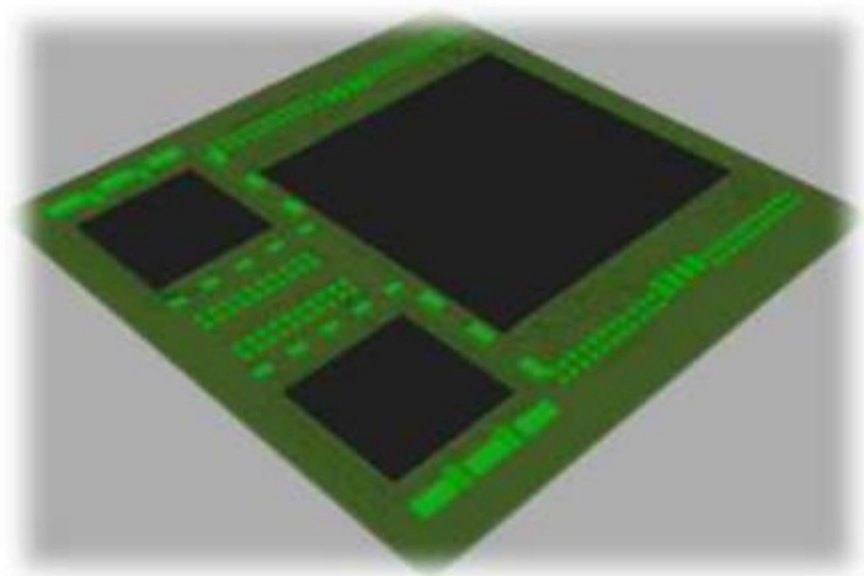
TV2 next gen





BGA 40 X 40 mm **1932** I/O
Pitch 1 mm
Flip Chip 25 X 25 mm **25921** I/O
Pitch 0.2 mm

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Questions

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